

WHAT IS CLAIMED IS:

1. A high-level synthesis method, comprising:
 - generating a CDFG (Control Data Flow Graph) based on an input file
 - describing a behavior of a digital circuit;
 - scheduling the CDFG by allocating each node of the CDFG generated in the CDFG generation, expressing contents of processing, to a time synchronized with a clock called a Step, based on the CDFG and a constraint condition of the digital circuit described in a constraint file;
 - generating allocation information representing how resources for constituting the digital circuit are allocated to respective nodes of the CDFG scheduled in the scheduling, based on resource-level layout information representing a layout of the resources, and based on circuit information representing a connecting relationship between the resources; and
 - outputting the circuit information generated in the allocation and circuit information generation.
2. The high-level synthesis method according to claim 1,
wherein the allocation and circuit information generation comprises:
 - generating initial allocation information representing how the resources are allocated to the respective nodes of the CDFG scheduled in the scheduling and initial circuit information representing a connecting relationship between the resources;
 - generating the resource-level layout information, based on the initial circuit information generated in the initial allocation and initial circuit information generation;
 - generating corrected allocation information representing how an allocation of the resources with respect to the respective nodes of the CDFG is changed and corrected circuit information representing how the connecting relationship between the resources is changed, based on the initial allocation information generated in the initial allocation and initial circuit information generation and the resource-level layout information; and
 - minutely correcting the resource-level layout information, based on the corrected circuit information generated in the corrected allocation and corrected circuit information generation, wherein
 - the corrected allocation and corrected circuit information generation, and the resource-level layout minute correction are performed repeatedly

until a predetermined standard is satisfied, and
in the corrected allocation and corrected circuit information
generation, corrected allocation information representing how an allocation of
the resources with respect to the respective nodes of the CDFG is changed
5 and corrected circuit information how the connecting relationship between
the resources is changed, are generated based on the resource-level layout
information and the corrected allocation information previously generated.

3. The high-level synthesis method according to claim 2, wherein the
10 allocation information contains hardware resource allocation information and
lifetime information of hardware resources.

4. The high-level synthesis method according to claim 1, wherein the
resource-level layout information is distance information of an inter-resource
15 connecting line.

5. The high-level synthesis method according to claim 1, wherein the
resource-level layout information is congestion degree information in a layout
region of an inter-resource connecting line.

20 6. The high-level synthesis method according to claim 1, wherein the
resource-level layout information is inter-macro connecting line information
expressed by any function composed of distance information of an
inter-resource connecting line and congestion degree information in a layout
25 region of an inter-resource connecting line.

7. The high-level synthesis method according to claim 1, wherein the
resource-level layout information includes a layout influence degree as a
coefficient.

30 8. The high-level synthesis method according to claim 2, wherein the
resources are allocated to the respective nodes of the CDFG so as to minimize
shared hardware resources in the initial allocation and initial circuit
information generation, and

35 an allocation of the resources with respect to the respective nodes of
the CDFG is changed so that hardware resource separately implemented are
shared in the corrected allocation and corrected circuit information

generation.

9. The high-level synthesis method according to claim 2, wherein the resources are allocated to the respective nodes of the CDFG so as to maximize shared hardware resources in the initial allocation and initial circuit information generation, and
5 shared hardware resources are allocated separately in the corrected allocation and corrected circuit information generation.
- 10 10. The high-level synthesis method according to claim 2, wherein, in the corrected allocation and corrected circuit information generation, an arrangement distribution variation in a layout region of memory resources is calculated, synthesis ease of a synchronization clock circuit is estimated based on the arrangement distribution variation in a layout region of the
15 memory resources, and sharing with high synthesis ease is selected when the memory resources are shared.
- 20 11. The high-level synthesis method according to claim 10, wherein the arrangement distribution variation in the layout region of the memory resources is a variation in number of the memory resources belonging to each region obtained by dividing the layout region into a plurality of regions.
- 25 12. The high-level synthesis method according to claim 10, wherein the arrangement distribution variation in the layout region of the memory resources is a total of variations calculated for each hierarchy obtained by dividing the layout region hierarchically.
- 30 13. The high-level synthesis method according to claim 2, wherein the resources are allocated to the respective nodes of the CDFG so as to maximize shared hardware resources in the initial allocation and initial circuit information generation,
35 the shared hardware resources are separately allocated in the corrected allocation and corrected circuit information generation, and
 the allocation and circuit information generation further includes changing the allocation by allowing the hardware resources divided in the corrected allocation and corrected circuit information generation to be shared with the hardware resources that are not shared in the initial allocation and

initial circuit information generation.

14. The high-level synthesis method according to claim 13, wherein the resource-level layout information includes a layout influence degree as a layout influence coefficient, and
 - 5 the corrected allocation and corrected circuit information generation and the allocation changing are repeatedly performed while the layout influence coefficient is corrected in stages.
- 10 15. The high-level synthesis method according to claim 2, wherein the resource-level layout information minutely corrected in the resource-level layout minute correction is further output in the outputting.